FREE BOOK: Component Design by Example

… A Step-by-Step Process Using VHDL with UART as Vehicle

Ben Cohen

Written in 2001, this book is unique in that it address, by example, the **processes** involved in specifying, implementing, and verifying a reusable soft component. Since then, technology has made significant progress in terms of capacity of chips, design and verification languages and libraries (SystemVerilog, UVM, SVA), and availability of IPs. However, what has remained somewhat constant is the generic need to write requirements and plans prior to proceeding to the actual RTL design and model verification. The requirements define what the chip should do, independently from the implementation. The architectural plan defines the general pieces of the design and their interconnections. The verification plan defines the approaches used for verification and validation to a high degree of confidence. And this where you may find this book useful: **How do you write these document?**

Another technology demonstrated in this book is the **OpenMore spreadsheet**. OpenMore (*Open Measure of Reuse Excellence*) is an assessment program developed by Synopsys and Mentor Graphics (in 2000) designed to enable a self-assessment of the reusability of commercial IP offerings. The OpenMORE assessment program contains 5 sections: 1) "Instructions", 2) "Soft IP Assessment", 3) "VSIA Cross-reference for Soft IP", 4) "Hard IP Assessment", and 5) "IP Information". This is an Excel spreadsheet with the sections in labeled tabs. In 2007 the work of VSIA was transferred to other consortia and standards bodies. I do not believe that the OpenMore speadsheet is used today, however its entries are very interesting and are worthy of consideration in evaluating the goodness of a design. The spreadsheet is included in the book (tar or zip file) (https://semiengineering.com/entities/vsia/)

Reading this book is best handled by thumbing through the document, getting familiar with its content, particularly the processes, and ignoring any VHDL code. I recommend this approach because the meat of this book is the processes. Needless to say that these processes need to be extended and enriched to your needs, but the core structure is there.

pdf: http://SystemVerilog.us/cmpts_design/cmpts_by_example.pdf
code, zip: http://SystemVerilog.us/cmpts_design/component_design_by_example_code_misc.zip
code, tar: http://SystemVerilog.us/cmpts_design/cmpts_design.tar

On a side note, my co-authors just published a very interesting book "**UnleashingUVM series, Just do it**" to facilitate the use of UVM. You may get a free copy at http://verifnews.org/jdi/

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For training, consulting, services: contact http://cvcblr.com/home
* http://goo.gl/JOfuEB SVA Handbook 4th Edition, 2016 ISBN 978-1518681448
* A Pragmatic Approach to VMM Adoption 2006 ISBN 0-9705394-9-5
* Using PSL/SUGAR for Formal and Dynamic Verification 2nd Edition, 2004, ISBN 0-9705394-6-0
* https://goo.gl/d10QHh Real Chip Design and Verification Using Verilog and VHDL, 2002 isbn 978-1539769712 [/url]
* Component Design by Example ", 2001 ISBN 0-9705394-0-1
* VHDL Coding Styles and Methodologies, 2nd Edition, 1999 ISBN 0-7923-8474-1
* VHDL Answers to Frequently Asked Questions, 2nd Edition ISBN 0-7923-8115

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1) https://verificationacademy.com/forums/systemverilog/vf-horizonspaper-sva-alternative-complex-assertions
2) http://systemverilog.us/vf/SolvingComplexUsersAssertions.pdf
3) "Using SVA for scoreboarding and TB designs"
http://systemverilog.us/papers/sva4scoreboarding.pdf
4) "Assertions Instead of FSMs/logic for Scoreboarding and Verification"
https://verificationacademy.com/verification-horizons/october-2013-volume-9-issue-3
5) SVA in a UVM Class-based Environment
https://verificationacademy.com/verification-horizons/february-2013-volume-9-issue-1/SVA-in-a-UVM-Class-based-Environment