What is verification of an FPGA/ASIC at RTL?
- Process of insuring design meets requirements
- Stimulus covers all important cases

How is verification done?
- Simulation
  - Subjecting the design to a variety of stimulus
    - Directed/random/constraint-random
  - Verifying that outputs meets requirements
    - Compare to pre-calculated results
    - Compared to expected results based on dynamic
  - Insure proper coverage
- Formal verification
  - Defining a set of assertions about the design
  - Formally verifying performance
  - Identifies uncovered states
Functional verification overview

What are the verification methodologies?

- **Simulation**
  - Custom-designed transaction-level modeling
    - New for every project/partition/variations/tests
    - Popular since 1990’s till now, used with VHDL and Verilog
  - Framework-based stimulus
    - Reusable across projects/partitions/variations/tests
    - VMM, UVM, ...
    - Supported my tools, e.g., Intelligent Testbench Automation
  - Functional assertions (over sequences)
  - Functional and data coverage

- **Formal verification**
  - RTL + assertions -> design quality
  - Assertion synthesis
  - RTL + simulation -> assertions (what RTL does) + coverage of design behavior
Methodology History

Vera → RVM

SystemVerilog → RVM

VMM → OVM

AVM → OVM

URM → OVM

OVM success forces Synopsys to open VMM

VMM1.2 includes OVM features and concepts. Users have to change a lot

Open Source

2005

2008

2011