3.1 ASYNCHRONOUS DATA INTO SYNCHRONOUS SYSTEM

Designers of digital systems are constantly confronted with the problem of synchronizing two systems that operate at different frequencies[24]. Such systems typically include the transfer of data between two subsystems, where the data source is not clock synchronized to the receiver. This data transfer may be over a data link, such as wires, fiber-optics, or satellite link. A Universal Asynchronous receiver transmitter represents such a model. There are also cases where circuit design techniques, such as ripple counter, will produce signals that are no longer in clock synchronization with the master clock. Other examples are rate converters where data is stored (in a FIFO) at one clock domain, and is extracted at a different clock domain.

Synchronization is very important in digital designs because synchronization bugs cause intermittent failures in board designs. These bugs can be frustratingly difficult to reproduce in the lab[25].

3.1.1 Metastability Definitions[26]

Metastability definitions are listed below to establish a baseline on terminologies.
Problem: Introducing an asynchronous signal into a digital (synchronized) system.

Metastable: A state between either "valid" digital logic state (an undefined voltage).

Digital Logic State: A defined range of voltages that indicates which logic level the device will switch to, or resides in. For TTL a logic low is {0 to 0 .7 volts}, a logic high is (2.4 to 5 volts).

Undefined Voltage: A voltage between the established logic level, either High or Low; (0.7 to 2.4 volts) from the example above.

Set-Up Time The time required for the input (data) signal to be valid before the incoming clock pulse.

Hold Time The time required for the input (data) signal to remain valid after the clock pulse.

Resolve Time: The amount of time the Flip Flop's output must return to a valid level before it is used. This is 1/(clock frequency). The output must be valid by the next clock.

Skew (Clock or data): The change in time of one signal compared to another, caused by timing delays or propagation delays (also see section 2.9). The timing differences developed by different devices performing the same function.

Ambiguity: The uncertainty in the amount of time it takes for a valid logic signal to change from one state to another.

Metastability Window: The specific length of time, during which both the data and clock should not occur. If both signals do occur, the output may go metastable.

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[24] Metastable Response in 5-V Logic Circuits, Texas Instruments, SDYA006 February 1997

[25] http://www.ednmag.com/ednmag/reg/1994/062394/13df2.htm
EDN -- 06.23.94 Keep metastability from killing your digital design

[26] http://www.interfacebus.com/Design_MetaStable.html

3.1.2 Metastable Condition Explained

Altera's application note 42 *Metastability in Altera Devices* provides an excellent explanation of metastability and mean time between the probable occurrence of two successive metastable events (Mean Time Between Failures, MTBF) reliability curves. The document is included on CD (*altera_an42_metastability.pdf*). The problem is that violating a flip-flop's setup or hold time can cause its output to become metastable. Figure 3.1.2-1 displays the metastability timing parameters. When a flip-flop is in metastable ("in Between") state, the output hovers at a voltage level between high and low, causing the output transition to be delayed beyond the specified clock-to-output delay (*Tco*). The additional time beyond *Tco* that a metastable output takes to resolve to a stable state is called the settling time (*Tmet*). Every transition that violates the setup and hold times results in a metastable output. The likelihood that a flip-flop enters a metastable state and the time required to return to a stable state varies on the process technology used to manufacture the device and on ambient conditions. Generally, the flip-flop quickly returns to a stable state.

The operation of a register is analogous to a ball rolling over a frictionless hill, as shown in Figure 3.1.2-2. Each side of the hill represents a stable state, and the top of the hill represents a metastable state. When a flip-flop's data input complies with the minimum setup (*Tsu*) and hold (*Th*) times, the output passes from one stable state to another without additional delay. Analogously, the ball travels over the hill within a specified time if given enough of a push.

However, when a flip-flop's data input violates the setup and hold time, the flip-flop is marginally triggered, and the output may not immediately resolve to either of the two stable states within the specified time. This marginal triggering can cause the output to glitch or to remain temporarily at the metastable state between the high and low levels, taking longer to return to a stable state. Either condition increases the clock transition to a stable output.

Figure 3.1.2-3[27] shows that the metastable state of the master flip-flop first generates a high level on the output of the slave. If the master then reverts to a stable state, a low level will appear again on the output of the flip-flop. The inverted signal shapes can be viewed in the same way. The phenomena shown here are described with reference to a bipolar circuit, but the same effects occur in CMOS and BiCMOS circuits.

[27] Metastable Response in 5-V Logic Circuits, SDYA006, February 1997 Texas Instruments

Additional Metastability information may also be found at:
http://www.verifarm.com/metastab.shtml

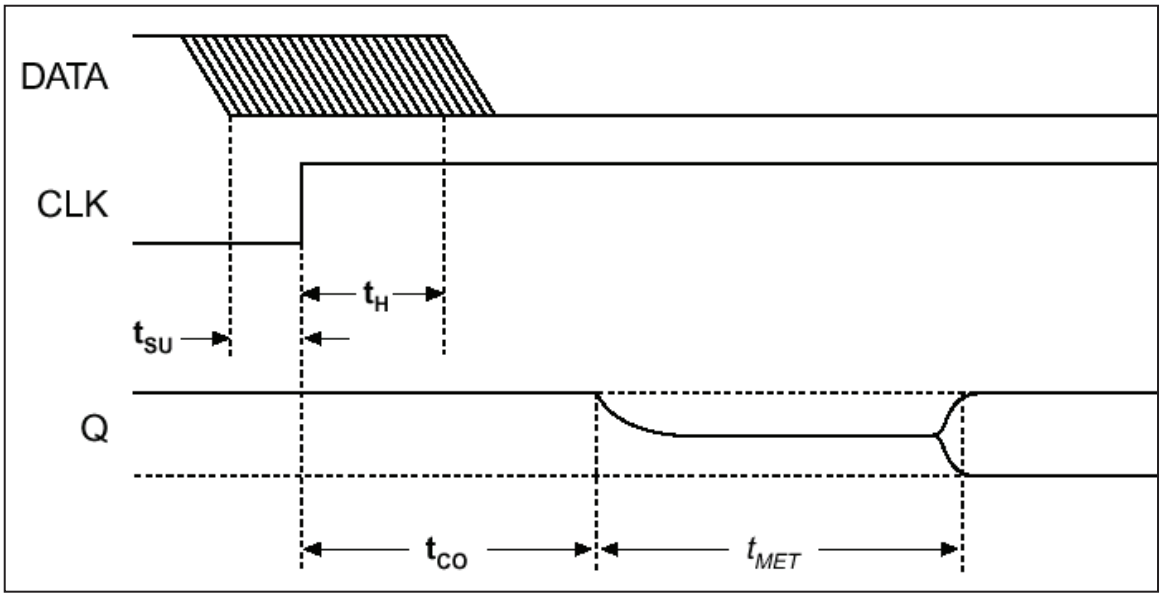

Figure 3.1.2-1 Metastability Timing Parameters

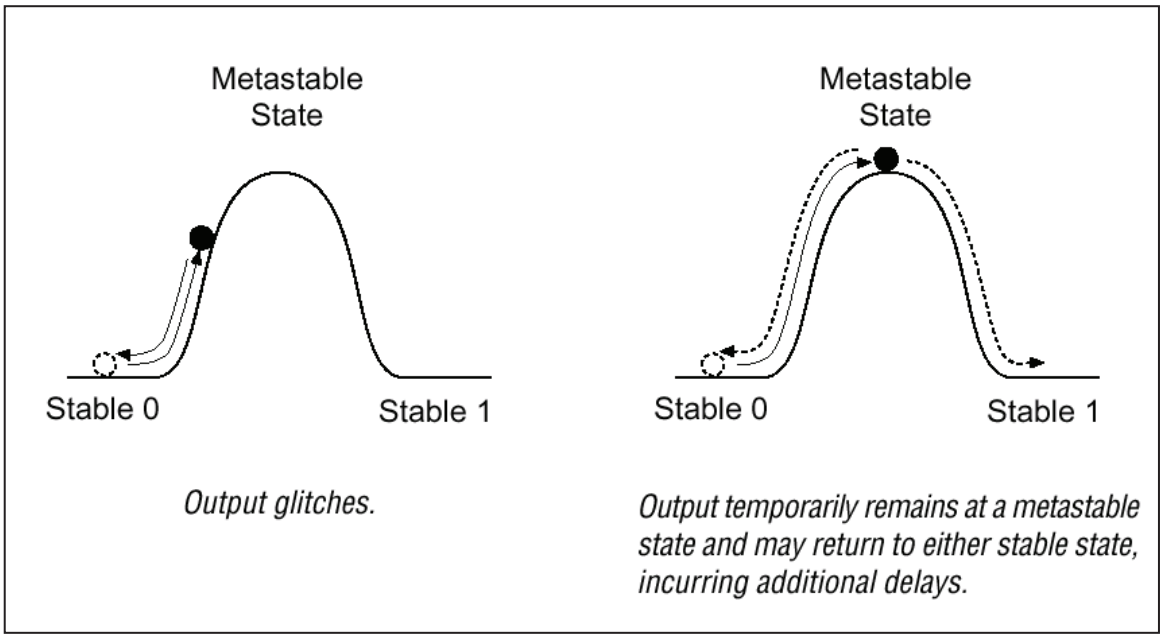

Figure 3.1.2-2 Effects of Violating Setup (Tsu) and Hold (Th) Requirements

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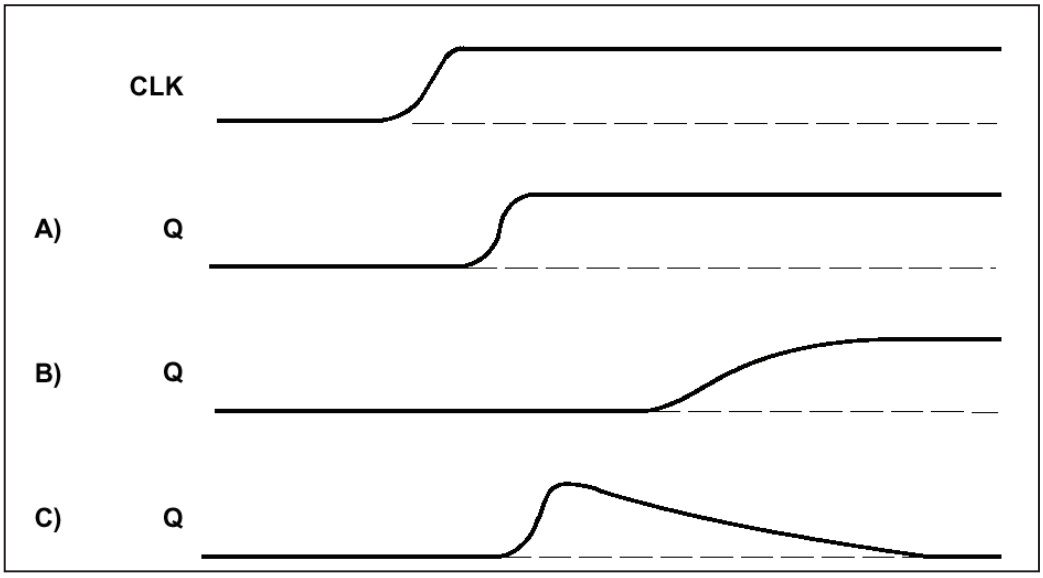

Figure 3.1.2-3 Different Output Signals in the Metastable State

3.1.2.1 MTBF in Single Stage Flip-Flop

The MTBF of a single-stage synchronizing flip-flop can be estimated by the following formula:

$$\mathrm{MTBF} = \frac{e^{(C_2 \times t_{MET})}}{C_1 \times f_{CLOCK} \times f_{DATA}}$$

t_{MET}	**Additional time for the signal to settle to a known state to prevent the propagation of undefined value to the rest of the system**
C1	**Metastability constant** **= 1.01×10^{-13} for Altera FLEX 10K** **= 2.98×10^{-17} for Altera MAX7000**
C2	**Metastability constant** **= 1.268×10^{10} for Altera FLEX 10K** **= 5.023×10^{9} for Altera MAX7000**

The above equation yield an MTBF of less than 0.71 hours for the Altera Flex 10K (and 1.13 hours for the Altera MAX 7000) at a 50 MHz clock rate, and 25 MHz data rate, and a 1 ns additional settling time, which cuts into the setup time (see Table 3.1.2.2).

One way to resolve **metastability** is to provide a window of excess setup time. This allows the input FF to bring itself out of **metastability** before the next clock edge. The more time allowed, the less likely it is to be metastable near the clock edge[28]. Thus, increasing the additional settling time to 2 ns boosts the single stage MTBF to 25.9 years for the FLEX10K, and to 196 years for the MAX700.

Figure 3.1.2.1 represents the output of a single-stage synchronizing flip-flop.

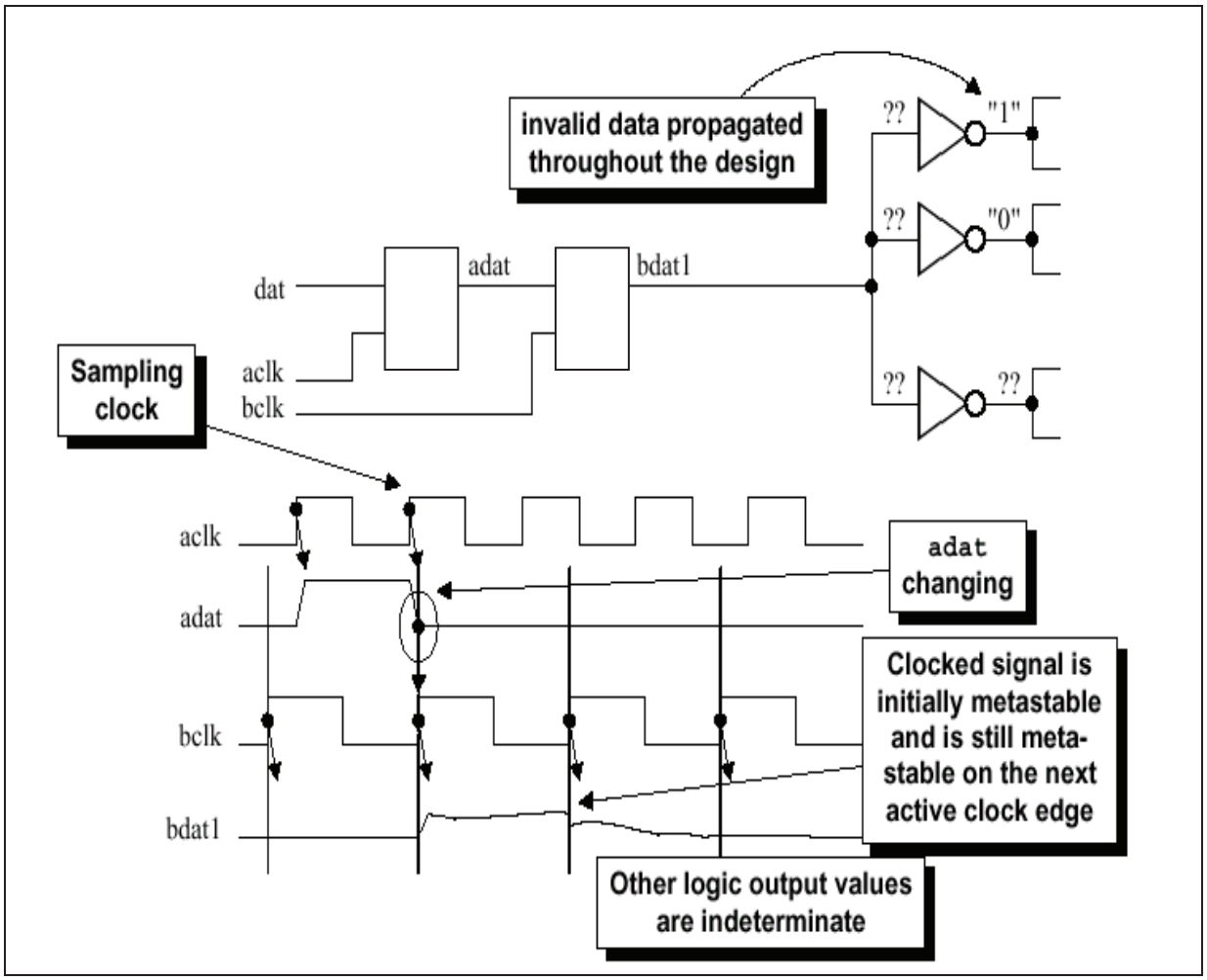

Figure 3.1.2.1 Output of a Single-Stage Synchronizing Flip-Flop, Metastable *bdat1* Output Propagating Invalid Data throughout the Design[29]

28 Xilinx Metastability Considerations, XAPP077 January, 1997 (Version 1.0) Application Note

29 *Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs*, Clifford E. Cummings, SNUG-2001,