
Real Chip Design and Verification Using Verilog and VHDL

Ben Cohen



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FOREWORD

Cadence Design Systems

Verilog and VHDL have been with us now for almost 20 years. During that time, we have watched them grow from esoteric new ways of specifying testbench and design functionality to the mainstay in any complex design methodology. Despite the wide usage and proliferation of HDL-based design methodologies, there is still much to be learned in this area for many people, from new designers just starting-out with HDLs to experienced engineers looking for ways to improve their productivity.

This new book by Ben Cohen is an invaluable addition to the existing literature on chip design using the Verilog and VHDL hardware description languages. As Ben notes in his Preface, the purpose of his book is not to teach either HDL, as there are already several books on the market that do an excellent job of describing and teaching the languages. However, as Ben also notes, a sound understanding of the HDL, though a requirement, is not sufficient. Understanding the HDL alone will not make you an expert logic designer, any more than learning C or C++ will make you an expert computer programmer.

One of the things that make this book particularly important is that it doesn't focus on just Verilog or VHDL, but rather on actual design and simulation using examples from both languages. No one actually designs using two languages at the same time, but more and more designers find themselves using IP in a different language or integrating their design with another one written in different language. In addition to driving the need for tools that support both languages, this is also driving the need for designers to understand both Verilog and VHDL at least well enough to be able to debug modules written in either language.

This book concentrates on common classes of hardware architectures and design problems, and focuses on the process of transitioning design requirements into synthesizable HDL code. Using his extensive, wide-ranging experience in computer architecture and hardware design, as well as in his training and consulting work, Ben provides numerous examples of real-life designs illustrated with VHDL and Verilog code. This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare. All code presented in the book is included on the companion CD, along with other information, such as application notes.

Ben also covers a critical aspect for any real-life testbench creation: the use of transaction-based verification techniques. Designs are too complicated to continue to validate them exclusively at the individual signal level. In order to both improve performance and ensure that the tests actually check intended behavior, designers need to create tests and verify results at the transaction level. The book includes a chapter covering on Verilog and VHDL transaction level testing while also referring to C++ based transaction level test tools such as the open-source *Testbuilder* (available at www.testbuilder.net).

Cadence Design Systems is proud that some of its leading digital verification products were used in the creation of this book. *HAL* was used for HDL analysis and lint checking, which provides a perfect static verification complement to the dynamic simulation featured in the rest of the book. The high-performance, mixed-language simulator *NC-Sim* was used for verifying all of the examples in the book and the results were shown using the *SimVision* GUI and debug environment.

This book is one of the best investments that a logic designer can make. We are certain that it will be of enormous value to all those involved in HDL-based chip design for years to come.

Rahul Razdan
Corporate Vice President - Systems and Functional Verification.
Cadence Design Systems, Inc.



FOREWORD *Synplicity, Inc.*

Ready, Fire, Aim! A humorous cliché, but uncomfortably applicable to describe the experience of many of our young digital designers. Most learn by doing, thus leaving a trail of first attempts that is less than impressive.

There is a gap in the education and training of many new entrants to our profession. The preeminent method of learning the practical techniques for HDL based digital design is to learn by experience. The consequence is that many designers become best capable later in their career. For many designers, this occurs at a time when their design skills are becoming less utilized as they progress down any number of career paths, such as architect, manager, application engineer, etc., leaving core design behind.

For those eager to learn the practical aspects of design, they often are left 'on their own'. There is a void in mentoring in engineering today. The designer must seek out information from books, from colleagues, from poking and probing through existing code to see what is typically done in the industry.

Universities often bolster the foundations of engineering, mostly theoretical, sometimes practical, but typically lagging industry. Thus, the recent graduate starts their career playing catch-up. Industry text books (as opposed to Academic textbooks) attempt to remain current but often are specific to a small slice of the design process -- such as books on HDL language semantics for simulation not synthesis, or books on design applications that ignore implementation. The designer is left to put the pieces together to form a whole.

In *Real Chip Design and Verification Using Verilog and VHDL*, Ben Cohen bridges gaps. He bridges the gaps in a designer's knowledge, he covers the gaps left by other texts. The focus on this book is to learn by example. The readers starting point is the macro elements and their implementation. Ben takes these elements, simulates them, synthesizes them, and leaves the reader with the ability to do the same. He defers giving bias to Verilog or VHDL, but rather acknowledges that both are in use, and thus the reader may utilize either or both in their career.

Ben bridges simulation and synthesis, and this acknowledges that implementation and verification must both be done in design. He then extends the discussion to more complex design objects, and discusses architectural tradeoffs in these components. These discussions extend to their impact for targeting FPGAs and ASICs, their final destination.

Ben continues to be a pragmatic author. His topics and writing are very accessible and pertinent to the engineering community he reaches. At Synplicity, we have benefited from Ben's knowledge of language and tools in his role as customer and author. Now you can too.

Andrew Dauman
Vice President, Corporate Applications Engineering
Sunnyvale, CA
October, 2001



PREFACE

Now that you know a hardware description language (HDL), where do you go from here? As a VHDL trainer and consultant, I experienced that many engineers understand the HDL from a software viewpoint, but do not know how to approach design problems. There is a fallacy that HDL is the panacea to all design issues, and that synthesis tools will perform the magic of translating the HDL into hardware. The reality is that synthesis is just a tool to help in the implementation of what is described. It is necessary that the authors of the HDL code understand the hardware architecture and implications of what is described. A proper HDL description of an incorrect or improper architecture does not necessarily yield a correct or optimum design. The following quotation, from a contributor in *comp.lang.vhdl* newsgroup, expresses this point in an interesting manner: *HDL (e.g., VHDL or Verilog), like any other EE design tool, assumes that the user has a working knowledge of electronics and digital design. I know many who are poor designers before learning HDL and remain poor designers after taking an HDL class.*

Real Chip Design and Verification Using Verilog and VHDL addresses the practical and real aspects of logic design, processes, and verification. It incorporates a collection of FPGA and ASIC design practices, and uses Verilog and VHDL as a tool for expression of the desired architectures. This book is not intended to teach either HDL, as there are several books specifically geared toward teaching the languages. However, it provides various architectural design primitives, applications, and verification techniques, along with design methodologies and common practices.

Logic design is an art that is learned, and often relearned by designers. There are several common classes of design problems and several common classes of hardware architectures including synchronization logic, counters, controllers, arithmetic elements, and storage elements. This book addresses those classes of designs with practical examples to expose the reader to variations in styles and approaches. The architectural issues, design decomposition, and HDL code in both VHDL and Verilog are discussed and demonstrated. Transaction-based testbenches with error injection methodologies demonstrate, by example, design verification techniques. Models used for this verification task include a counter and an EDAC (error detection and correction) logic with a RAM.

This book is intended as a training book in conjunction with an HDL class as a means to demonstrate the transition of design requirements into an HDL design. Specifically, it demonstrates by example the following:

1. Styles of hardware architectures.
2. Logic design architectural decomposition process and the translation of the architectures into HDL.
3. HDL coding styles.
4. Verification techniques with HDL using transaction-based methodologies.

Cadence *NC-Sim* simulator and *HAL* analysis and lint checking tools were used because of their levels of efficiency, accuracy, and maturity. Cadence represents a vendor that is a leader in the EDA industry. Synplicity *Synplify Pro*® FPGA synthesis tool was also extensively used because Synplicity is recognized as a vendor of advanced, efficient, and easy to use synthesis tools targeted for FPGAs, and now ASICs. Even though these specific tools were used, almost all of the information is tool independent.

Chapter 1 provides an overview of the architectural decomposition process, and presents the classes of hardware designs. **Chapter 2** presents fundamental architectural elements used in the construction of designs. These include flip-flops, latches, synchronous edge detector, application of both edges of the clock, registers, counter styles (*e.g.*, *Binary*, *One-Hot*, *Gray*, *LFSR*, *Johnson*), memories including ROM, RAM, FIFO, and Error Detection and Correction (EDAC) logic. A trigonometric function defined in C, but implemented in HDL as a ROM, is also demonstrated. This chapter also addresses the importance of understanding the cell primitives and FPGA architecture including the clocking features of ASICs and FPGAs. Topics on clocking schemes and phase lock loops are discussed. **Chapter 3** addresses the synchronous/asynchronous aspects of the real world, and methods to resolve those issues. Metastability is explained, MTBF calculations are defined, and solutions in the handling of metastability are presented. The design of an asynchronous FIFO is demonstrated. The topic of crossing clock domains is also presented. **Chapter 4** addresses the verification issue and presents through two examples the transaction-based verification methodology. The topic of forcing design errors is also demonstrated in those examples, including the verification of a loadable counter and an EDAC model for a thirty-two-bit wide memory. **Chapter 5** focuses on control machines and uses a very simple CPU design to demonstrate implementation methodologies with FSM and microprogrammed solutions. **Chapter 6** addresses arithmetic intensive machines. It explains the application of SIGNED and UNSIGNED types in HDL. Verilog 1995/2001 type issues are demonstrated. **Chapter 7** explains and demonstrates mixed mode simulations and synthesis. **Chapter 8** presents a discussion on minimizing design errors and addresses miscellaneous design issues. **Chapter 9** compares Verilog to VHDL to enable users of one discipline to understand the language differences and nuances of the other discipline. It also provides Verilog coding style guidelines for VHDL and Verilog users.

All HDL code described in the book is on a companion CD. All code was verified and simulated with *NC-Sim version v03.30.1*¹. All synthesizable code was synthesized with *Synplify Pro*[®] *version 6.2.4*². The CD also includes application notes and files of practical use that were collected over a period of several years. EMACS editor for Windows, along with VHDL and Verilog modes is on CD. The CD includes data sheets and additional information on Synplicity's product line, and excellent Cadence's Verilog reference and HDL simulation documentation.

This book is intended for:

1. **Engineers.** Book provides classes of architectural examples and decomposition into HDLs. Engineers are better at copying and improving upon what is done, than from starting from scratch. This book will provide a head start in these processes.
2. **Trainers.** This book provides the focus of an advanced hardware design class using HDLs. Emphasis is on architecture, processes, methodologies, and style.
3. **College students.** Book demonstrates the hardware architectural processes.

A list of Verilog books that are often recommended includes:

Verilog HDL : A Guide to Digital Design and Synthesis, Samir Palnitkar, 396 pages, Prentice Hall 1996, ISBN: 0134516753

Verilog HDL Synthesis, A Practical Primer, J. Bhasker, 236 pages, Star Galaxy Publishing, ISBN 0-9650391-5-3

A Verilog HDL Primer, Second Edition, J. Bhasker, 1999, Star Galaxy Publishing, ISBN 0-9650391-7-X.

The Verilog Hardware Description Language, Fourth Edition, Thomas, D . E . / Moorby, Philip R , 354 Pages, Kluwer Academic Publishers 1998, 354 Pages

For information about the new features of Verilog, I recommend the book *VERILOG 2001, A Guide to the New Features of the Verilog Hardware Description Language*, Stuart Sutherland, 2002, Kluwer Academic Publishers, ISBN 0-7923-7568-8

¹ Cadence Design Systems, Inc. <http://www.cadence.com/>

NC-Sim is available on several platforms including Win98, Win2000, WinNT4.0, Linux, Unix, HPPA.

For a guided tour of the Cadence VHDL and Verilog Desktop simulator please go to following page.

<http://www.orcad.com/product/simulation/hdlsim/>

² Synplicity <http://www.synplicity.com>

For VHDL, I second Janick Bergeron's recommendation³ for the book *VHDL Coding Styles and Methodologies, 2nd Edition*, 1999, Kluwer Academic Publishers, ISBN 0-7923-8474-1.

Another highly recommended book for VHDL is *The Designer's Guide to VHDL, 2nd Edition*, Peter J. Ashenden, 740 pages, Morgan Kaufmann Publishers, ISBN 1558606912

For verification, the book *Writing testbenches: Functional Verification of HDL Models*, Janick Bergeron⁴ Kluwer Academic Publishers, ISBN 0-7923-7766-4 is recognized as a standard.

³ *Writing testbenches, Functional verification of HDL models*, Janick Bergeron, Kluwer Academic Publishers 2000

⁴ <http://janick.bergeron.com/>

About The CD

Table 1 summarizes the contents of the enclosed CD.

Table 1 Contents of Enclosed CD

Chapter 2


MODEL	FIGURE	DESCRIPTION
ch2/ff_reset.v	2.1-1	Verilog Resettable Flip-Flop
ch2/ff_reset.vhd	2.1-2	VHDL Resettable Flip-Flop
ch2/latch.v	2.2-1	Verilog Latch
ch2/latch.vhd	2.2-2	VHDL Latch
ch2/oneshot.v	2.3-2	Verilog Code for Edge-Detect and Testbench
ch2/oneshot.vhd	2.3-2	VHDL Code for Edge-Detect and Testbench
ch2/negposff.v	2.4.2-1	Using Negative Edge of Flip-flop to Clock Data, and using Positive edge of Clock to Output Data to System
ch2/ser2parallel.v	2.5.1-1	Simple Serial to Parallel Converter with External Synchronization
ch2/ser2parallel.vhd	2.5.1-2	Simple Serial to Parallel Converter with External Synchronization
ch2/parallel2ser.v	2.5.2-1	Verilog Parallel to Serial Converter
ch2/parallel2ser.vhd	2.5.2-2	VHDL Parallel to Serial Converter
ch2/regfile.v	2.5.3-1	Register File Inference in Verilog
ch2/regfile.vhd	2.5.3-2	Register File Inference in VHDL
ch2/counter.v	2.6.1-1	Binary Verilog Counter
ch2/counter.vhd	2.6.1-2	Binary VHDL Counter
ch2/counterun.vhd	2.6.1-4	Counter Example with Numeric_Unsigned Package
ch2/dncounter.v	2.6.2-1	Verilog Model of a Loadable Down-Counter
ch2/dncounter.vhd	2.6.2-2	VHDL Model of a Loadable Down-Counter
ch2/freerundncntr.v	2.6.3-2	Down-Counter Configured as a Free-Running Counter
ch2/ freerundncntr.vhd	2.6.3-3	Down-Counter Configured as a Free-Running Counter
ch2/counter5.v	2.6.4-1	Simple 5-Bit Up-Counter with Terminal Count




ch2/counter5.vhd	2.6.4-2	Simple 5-Bit Up-Counter with Terminal Count
ch2/lfsr4.vhd & ch2/TestLFSR_tb.vhd	2.6.5-1	Simulation of Four-bit LFSR
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ch2/lfsr4count.v	2.6.5-5	Verilog Model for 4-bit LFSR Counter
ch2/lfsr4count_tb.v	2.6.5-5	Verilog Testbench for 4-bit LFSR Counter
ch2/counter1hot.v	2.6.6-1	Verilog Model of One-Hot Counter
ch2/counter1hot.vhd	2.6.6-2	VHDL Model of One-Hot Counter
ch2/counter1hotsafe.v	2.6.6-4	Verilog Model of Safe One-Hot Counter
ch2/counter1hotsafetb.v	2.6.6-6	Verilog Model testbench for the safe One-Hot Counter
ch2/counter1hotsafe.vhd	2.6.6-7	VHDL Model of Safe One-Hot Counter
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ch2/gray2bin.vhd	2.6.7.2-3	Working Gray-to-Binary VHDL Model
ch2/gray2bin.v	2.6.7.2-4	Parameterized and correct gray-to-binary Verilog model
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ch2/bin2gray.vhd	2.6.7.3-2	VHDL Binay to Gray Converter
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ch2/graycntr_lookup.v	2.6.8-10	Verilog Gray Code Counter lookup style
ch2/graycntr.vhd	2.6.8-1	VHDL Gray Code Counter with binary output
ch2/graycntr_lookup.vhd	2.6.8-9	VHDL Gray Code Counter lookup style
ch2/graycntr_tb.v	2.6.8-5	Verilog Testbench for the Graycode Counter
ch2/graycntr_tb.vhd	2.6.8-7	VHDL Testbench for the Graycode Counter
ch2/Johnson.v	2.6.9-1	Verilog Johnson Counter with terminal count
ch2/Johnson.vhd	2.6.9-4	VHDL Johnson Counter
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ch2/rom6.vhd	2.7.1-5	VHDL ROM Model
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IEEE (Arithmetic Packages)		numeric_std.vhd numeric_signed.vhd numeric_unsigned.vhd numeric_bit.vhd numeric_extra.vhd std_logic_1164.vhd std_logic_arith.vhd std_logic_unsigned.vhd std_logic_misc.vhd std_logic_signed.vhd
DRAGONFLY		The DRAGONFLY micro core has been designed as a small (less than 4K gates), fast and programmable core, to be used in an ASIC or a FPGA, in areas such as serial communication management (UART, Smart cards controllers, LDC drivers, I ² C controllers, SPI controllers), on-chip test and debug of complex blocks, intelligent DMA, FLASH controllers, audio-rate SDRAM controllers, and so on. VHDL Models and documentation.
DSP		DSP (DEMANDING SPACE-BASED PROCESSING!) THE PATH BEHIND AND THE ROAD AHEAD Dr SM Parkes, Applied Computing, University of Dundee, Dundee, DD1 4HN, Scotland, UK PDF Document
CliffCummings		www.sunburst-design.com Sunburst Design, Inc. Home Page www.sunburst-design.com/cliffc Cliff's bio page www.sunburst-design.com/papers Cliff's papers web page (to download papers, go to Cliff's papers web page and select one of the papers listed) - Coding And Scripting Techniques For FSM Designs With Synthesis-Optimized, - Glitch-Free Outputs Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - Nonblocking Assignments in Verilog Synthesis, Coding Styles That Kill! - Verilog-2001 Behavioral and Synthesis Enhancements RTL Coding Styles That Yield Simulation and Synthesis Mismatches Verilog Training
RamLib		Free IP, Free RAM Models and documentation (Ram and FIFO in VHDL)
risc8		Free IP, The Free-RISC8 is a Verilog synthesizable model of a simple 8-bit microcontroller. Ans_RISC8_Core – VHDL Model
6502		FREE IP, FREE-6502 in VHDL

8051		VHDL 8051 processor
HDL_Info	Verilog_vs_vhdl  VerilogHDL Coding_Motorola Verilog-Mode vlogfaq1,2,3 vhdlfaq1,2,3,4 Vhdl-syntax_93 Vhdl-syntax_93 VHDL.hlp	VHDL & Verilog Compared & Contrasted Plus Modeled Example Written in VHDL, Verilog and C Douglas J. Smith, VeriBest Incorporated. Please fetch from http://www.angelfire.com/in/rajesh52/verilogvhdl.html Verilog HDL Coding, Semiconductor Reuse Standard, Motorola Verilog-Mode for emacs (auto) Verilog FAQ VHDL FAQ VHDL Syntax VHDL Help
Synplicity	Launch.exe 	Get Synplify & Synplify Pro Synplicity University Program Literature Synplify Datasheet Synplify Pro Datasheet Synplify/Amplify Family Brochure Success with MindTree Consulting Success with Sonus Networks Synplify web page Synplify Pro web page
Cadence	 vlogrefTOC.html ncvlogTOC.html ncvlogPN ncvhdlTOC.html ncvhdlPN nccoexpNTOC.	See http://www.cadence.com/ http://www.cadence.com/products/index.html Verilog-XL Reference, Product Version 3.3 Cadence NC-Verilog Simulator Help, Product Version 3.3 Cadence NC-Verilog Simulator Product Notes, Version 3.3 Cadence NC-VHDL Simulator Help, Product Version 3.3 Cadence NC-VHDL Simulator Product Notes, Version 3.3 Cadence NC-Sim Mixed Language Simulator Notes, V 3.3 For a guided tour of the Cadence VHDL and Verilog Desktop simulator http://www.orcad.com/product/simulation/hdlsim/

CPU-Design-HOWTO	CPU-Design-HOWTO.html 	<i>The document has URL links to help students understand how a CPU is designed and manufactured.</i>
CVS-RCS-HOWTO.html	CVS-RCS-HOWTO.html	<i>This document is a "practical guide" to very quickly setup CVS/RCS source code control system</i>
C++Programming-HOWTO	C++Programming-HOWTO.html	<i>This document provides a comprehensive list of C++ URL pointers, links to C++ online textbooks, and programming tips on C++.</i>
Emacs-Beginner-HOWTO	Emacs-Beginner-HOWTO.html	<i>This document introduces users to the Emacs editor</i>
emacs_tshell		Emacs and Tshell + GNU tools for PC Windows 9X/NT/2000
leon-2.2		<i>From http://www.estec.esa.nl/wsmwww/leon/ The LEON core is a <u>SPARC*</u> compatible integer unit developed for future space missions. It has been implemented as a highly configurable, synthesizable VHDL model. To promote the SPARC standard and enable development of system-on-a-chip (SOC) devices using SPARC cores, the <u>European Space Agency</u> is making the full source code freely available under the <u>GNU</u> LGPL license.</i>
OpenMore		OpenMore spreadsheet for grading of designs
sutherland-hdl.html		Link to Verilog 2001, Sutherland HDLCON paper Sutherland HDL, Inc Links to Verilog books and web sites, on-line Verilog reference, training, etc..

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⁵ <http://www.synplicity.com/>

⁶ <http://www.cadence.com/>

⁷ <http://www.sunburst-design.com/> (*Expert Verilog, Synthesis and Verification Training*)

⁸ <http://www.memecdesign.com/>

⁹ <http://rk.gsfc.nasa.gov/>



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Express my Long Hours with a Laptop in the Creation of HDL Books**

About the Author

Ben Cohen is currently an HDL language trainer and consultant. He has technical experience in digital and analog hardware design, computer architecture, ASIC design, synthesis, and use of hardware description languages for modeling of statistical simulations, instruction set descriptions, and hardware models. He applied VHDL since 1990 to model various bus functional models of computer interfaces. He authored *VHDL Coding Styles and Methodologies*, first and second editions, and *VHDL Answers to Frequently Asked Questions*, first and second editions, and *Component Design by Example*. He was one of the pilot team members of the VHDL Synthesis Interoperability Working Group of the Design Automation Standards Committee who authored the *IEEE P1076.6 Standard for VHDL Register Transfer Level Synthesis*. He is currently a member of the *VHDL* and the *Verilog Synthesis Interoperability Working Group of the Design Automation Standards Committees*. He taught several VHDL training classes, and provided VHDL consulting services on several tasks.

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